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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,081	08/22/2003	Ravindraraj Ramaraju	SC12814TC	9610

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EXAMINER	
WELLS, KENNETH B	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 07/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,081	RAMARAJU ET AL.	
	Examiner	Art Unit	
	Kenneth B. Wells	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 8/22/03.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *2,7 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,8-19 and 21-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/22/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Applicant's election of species A (Fig. 2) is acknowledged, with claims 1, 3-6, 8-19 and 21-26 reading thereon. Claims 2, 7 and 20 are withdrawn from consideration.

2. Claims 1, 3-6, 8-19 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, lines 4-5, the recitation of providing the first and second intermediate signals "at the complementary logic states" is incorrect, and thus misdescriptive of the invention shown in instant Fig. 2. As illustrated therein, the first and second intermediate signals are opposite to the recited complementary logic states of the input signals DATA and DATAB (note the same problem in claim 6). As a minor point in claim 1, the term --both-- should be inserted after the word "providing" on line 11 for clarity. Also for clarity in claim 1 on lines 11-13, applicant should insert some recitation of where/to what the first and second input signals are "provided" so as to make it more clear what is meant at lines 11-13 of claim 1. Also incorrect in claim 1 is the recitation at lines 14-16 of enabling clock "inputs", i.e., as shown in instant Fig.

2, there is only a single clock input of the first and second clocked inverters.

Claim 3 is indefinite because it also appears to be incorrect, i.e., if the clocked input (gate of FET 226) is disabled, then it would appear that neither of clocked inverters 220, 230 will perform any inverting function. Note the same type of problem in claim 5.

Claim 16 is indefinite because it cannot be determined if additional circuit elements were intended to be set forth (in view of the semicolon at the end of line 9) of if this is supposed to be the end of the claim.

As another minor point, the word "inverters" in claim 26, line 5 is misspelled (or at least is inconsistent with the previous spelling of this term).

3. Claims 1 and 3-5 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

It cannot be determined from the disclosure how the claimed timing is achieved, i.e., how the circuit of instant Fig. 2 can

provide the function set forth on lines 12-17 of claim 1. For example, how is the "providing both the first and second input signals at the same logic state" achieved? Moreover, how is the "enabling the clock input of the first and second clocked inverters prior to providing the first and second input signals at the same logic state" achieved?

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-6, 8-19 and 21-26, to the extent understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Shiratake.

Note Fig. 24 of this reference, where the Q and/Q input signals correspond to applicant's DATA and DATAB; the clocked inverters M11,M13 and M12,M14 correspond to applicant's elements 220,230; the clocked inverters M3 and M4 correspond to applicant's elements 200, 210; and the clocking of the two pairs of inverters shown in Fig. 24 of Shiratake (enabling the clock input of the first and second clocked inverters prior to

providing the first and second input signals at the same logic state) is met by the action of complementary clock signals clk and /clk being applied to the clock inputs (gates of NMOSFETs M10 and M1) of the two pairs of inverters.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Note the various embodiments of Aoki, which are also to seen to anticipate at least the independent claims of the instant application.

6.Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth B. Wells whose telephone number is (571)272-1757. The examiner can normally be reached on Monday through Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached at (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval

(PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kenneth B. Wells
Primary Examiner
Art Unit 2816

July 22, 2005